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The ARF18 decoder microcontroller has to be associated to an ARF4001 receiver module. Its purpose is to decode the frames emitted by the 2, 4 and 8-button remote controls of the ARF18 range.

On receipt of these encoded frames, it decodes them then compares them with those previously stored in the learning phase. If applicable it activates the outputs associated to this order. There are 24 accessible outputs arranged in 3 banks.

It manages the different operating modes - the programming is the man-machine interface.

1 - Technical data

Supply voltage: 5V
 Microprocessor: 68HC705C9ACFN

Ref.	Number	Signal	Description
RST/	1	Input	Reset: Active at low level. A logic level 0 on this input causes initialisation of the microcontroller.
IRQ/	2	Input	Interrupt input
VPP	3	Power	Programming voltage. Connect to VDD, in no case to VSS
NC1	4		
PA7	5	Out	Output 8 activated if the frame received and recognized has been assigned to it
PA6	6	Out	Output 7 activated if the frame received and recognized has been assigned to it
PA5	7	Out	Output 6 activated if the frame received and recognized has been assigned to it
PA4	8	Out	Output 5 activated if the frame received and recognized has been assigned to it
PA3	9	Out	Output 4 activated if the frame received and recognized has been assigned to it
PA2	10	Out	Output 3 activated if the frame received and recognized has been assigned to it
PA1	11	Out	Output 2 activated if the frame received and recognized has been assigned to it
PA0	12	Out	Output 1 activated if the frame received and recognized has been assigned to it
PB0	13	Out	Output A activated if the frame received and recognized has been assigned to it
PB1	14	Out	Output B activated if the frame received and recognized has been assigned to it

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			assigned to it. Accessible only in monostable mode.
PB2	15	Out	Output C activated if the frame received and recognized has been assigned to it. Accessible only in monostable mode.
PB3	16	Out	Power command: Output at high state 260 ms after the decoder has left "learning" mode. This output is used to suppress the power on the output stages when programming the links. NB: same timing as on PC3
NC2	17		
PB4	18	Output	Unused. To be connected to NC2
PB5	19	Out	Hold: This output supplies an impulse on establishment of a monostable output and on its release.
PB6	20	Input	Serial input of the information emitted by a remote control for processing by sampling. To be connected to TCAP [41].
PB7	21	Mem	CS mem2: unused
VSS	22	Power	Reference for signals and power supply
NC	23		
PC7	24	Mem	CS mem1: output for selection of the memory to be connected to the CS pin of the EEPROM memory used.
PC6	25	Output	Unused
PC5	26	Out	Error led. Output at low state as soon as an error occurs in a learning phase.
PC4	27	Out	Validate led. Output at low state as soon as a validate or a delete in "learning" mode is correctly completed.
PC3	28	Out	Mode led. Output at low state 260 ms after the decoder has entered "learning" mode. This output is used to light a mode display led. NB: same timing as on PB3
PC2	29	Output	Unused
PC1	30	Input	Mode input: A high level on this input sets the decoder to Learning mode. A low level sets it to normal operating mode.
PC0	31	Input	Reset input: In normal mode a high level on this input cuts all the active outputs. In programming mode a high level on this input deletes all or part of the programming.
PD0	32	Input	Selection input: scans only in programming mode. Enables the outputs to be assigned to be scrolled either one after the other or page by page.
PD1	33	Input	
PD2	34	Mem	MISO: to be connected to the EEPROM memory data output
PD3	35	Mem	MOSI: to be connected to the EEPROM memory data input
PD4	36	Mem	SCK: to be connected to the EEPROM memory clock signal
PD5	37	Input	

TCMP	38	Out	Unused
NC3	39		
PD7	40	Output	Unused. To be connected to NC3
TCAP	41	Input	Input to collect information emitted by a remote control for decoding. To be connected to PB6 [20].
OSC2	42		4MHz quartz connection. Not connected if an external clock is used.
OSC1	43		Connection of a 4MHz quartz or an external CMOS clock at this same frequency.
VDD	44	Power	+5V power supply

3 - EEPROM memory

It is imperative to associate an EEPROM memory to the microcontroller. This memory is used for learning the remote control button – output associations. A button is identified by 3 bytes. Each output can be activated by a maximum of 8 buttons. A minimum of 768 bytes (24 x (3+1) x 8) i.e. 6 kbits is therefore required. The decoder memory driver is written to operate with an 8 kbit microwire EEPROM with the following wiring:

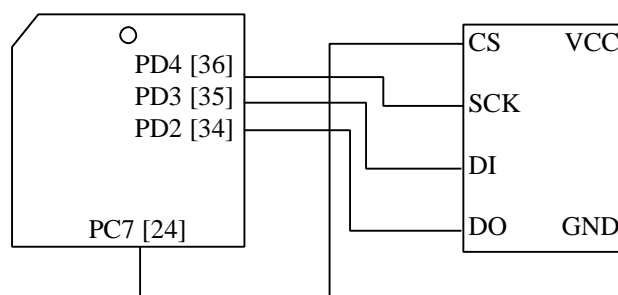
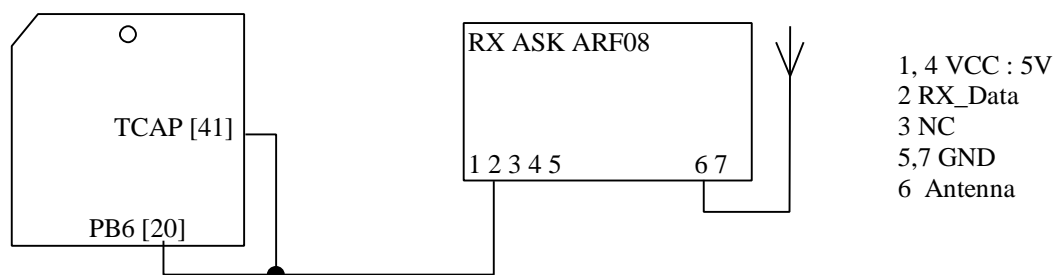


Figure 1 : EEPROM wiring

4 - User inputs

4.1 Receiver connection

This decoder is designed to work with ADEUNIS ARF 18 remote controllers. It should be used with the ARF08 ASK receiver.



For more information please consult the ARF08 users' guide.

4.2 AUTO/PROG [PC1]:

A low level on this input sets the decoder to programming mode. This is link edit mode. Operation in this mode is described by the status controller below:

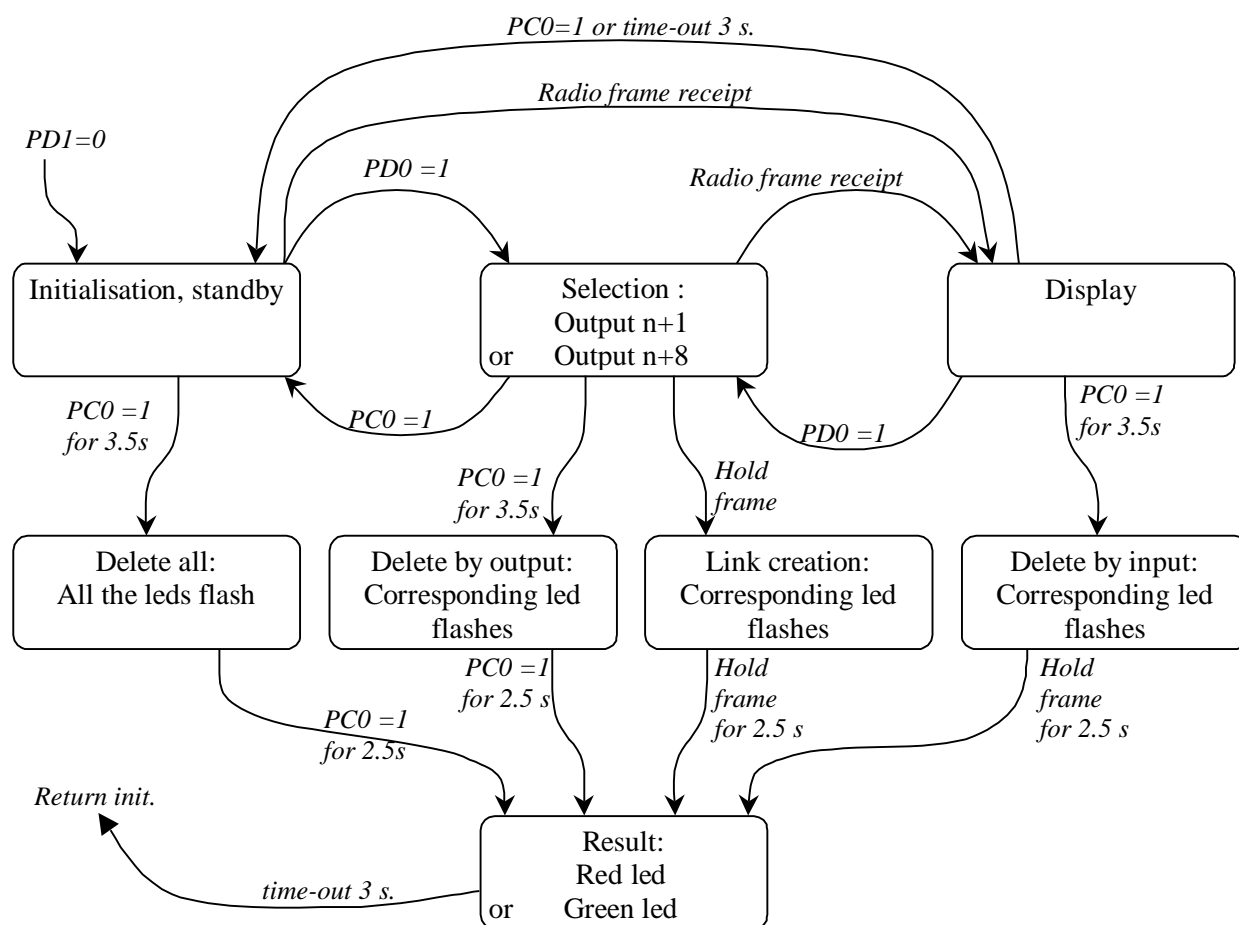


Figure 2: Status controller in programming mode

A high level on this input sets the decoder to automatic mode. Operation of the decoder then depends on the learning operations performed in programming mode.

4.3 Mode [PD1]:

This input configures the operating mode of all the outputs. At low level the outputs are in bistable mode - they change state each time an associated button is activated. In this mode the outputs are stored in case of a power failure or if programming is performed. They are restored when the power supply returns or when returning to auto mode. At high level the outputs are in monostable mode - they are activated so long as an associated button is activated.

4.4 Selection [PD0]:

In programming mode a high level on this input of a duration comprised between 120 ms and 1.6 s causes a switch from one output to the next output; e.g. from 4A to 5A or from 8B to 1C. A long high level, greater than 1.6 s, in programming mode goes on to the next page, e.g. from 7A to 7B.

In normal mode this input has no effect.

4.5 RESET [PC0]:

In programming mode, a high level on this input of a duration comprised between 120 ms and 6.1 s causes the current selection to be deleted without any action on the EEPROM memory.

A high level of a duration greater than 6.2 s causes a delete in the memory. If an input was selected deletion of all the links proper to this input will take place, if no input was selected deletion of the entire EEPROM memory will be performed.

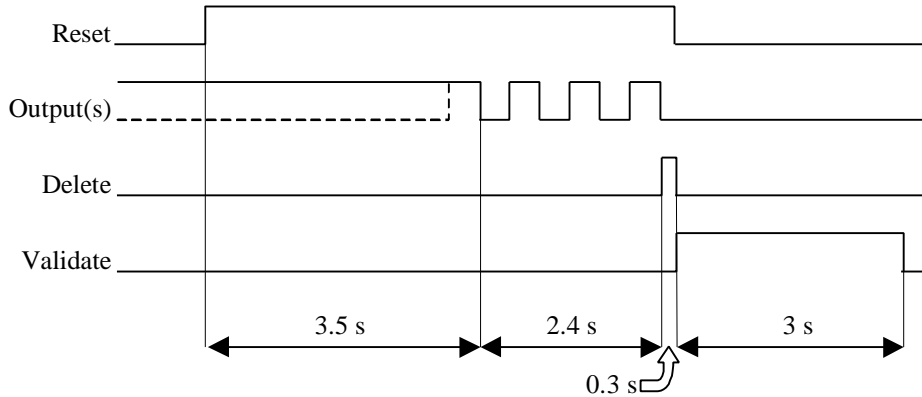


Figure 3: timing diagram - total deletion or delete by output

N.B.: if the output was selected in programming mode by a short press on a remote control button, a high level on the RESET input causes flashing of the output involved during which the radio frame has to be emitted to delete all the links proper to this button.

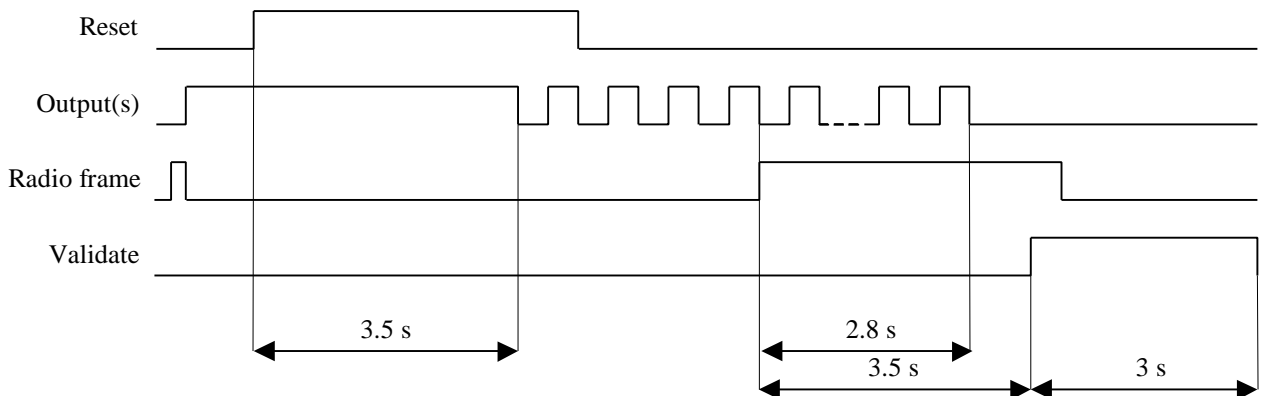


Figure 4: timing diagram by input

In normal mode a high level on this input of a duration greater than 120 ms cuts all the active outputs, without any action on the EEPROM memory.

5 - Outputs

5.1 Error display PC5

This output has the same timing as the validate output used to display the end of a learning operation. The causes of error are as follows:

- ✂ Assignment of a button to outputs on different pages from one another.
- ✂ Assignment of more than 8 buttons to the same output.
- ✂ When the memory is empty in auto mode.

5.2 Useful outputs PA0 to PA7 and PB0 to PB2

PA0 to PA7 are the eight outputs directly usable to control a relay, a transistor etc. Several of them can be active at the same time.

PB0 to PB2 are three outputs able to be used to perform switching to 24 outputs. Only one of these three outputs is active at any one time. In bistable mode only the output PB0 is activated.

The wiring example opposite also uses the output PB3 for disabling the outputs in programming mode. (OE : output enable)

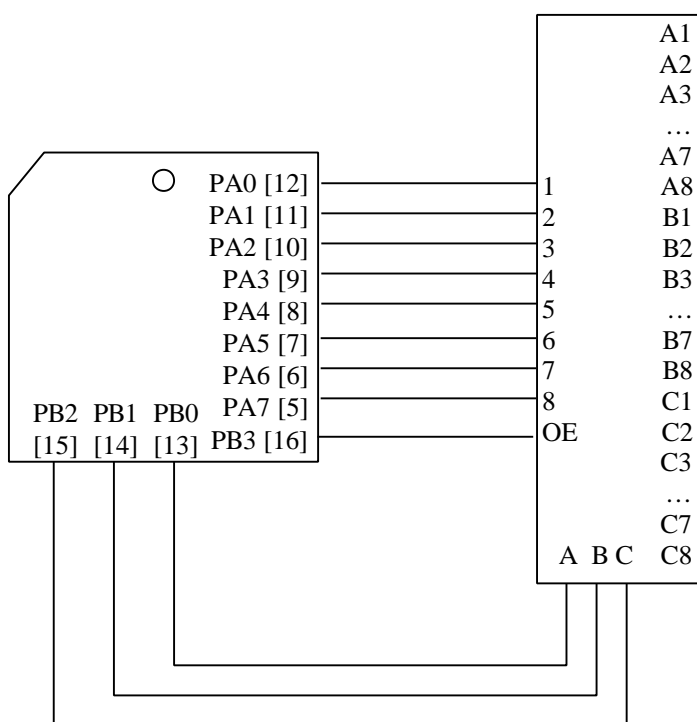


Figure 5: Wiring - 24 outputs

5.3 Hold output PB5

Like the signal PB3 above, there exists a complementary signal for management of the outputs. The signal PB5 supplies an impulse of 2.5 μ s on occurrence and disappearance of the hold pattern in a radio frame. This output is of no interest other than in monostable mode.

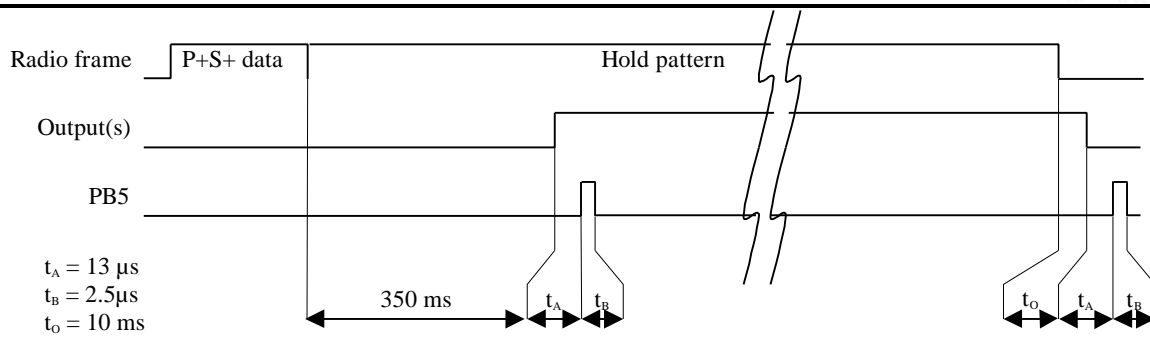


Figure 6: PB5 timing

N.B. The time of 350 ms is the time for processing the received frame and for searching for an occurrence in the EEPROM memory.